

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

C. Amendments to the Claims.

1. **(Original)** A semiconductor integrated circuit, comprising:

an inductor on a substrate;

5 a first metal layer inside the inductor when viewed from a direction perpendicular to a surface of the substrate, a lower surface of the first metal layer being no higher than a lower surface of the inductor;

10 a ferromagnetic substance layer on the first metal layer, a lower surface of the ferromagnetic substance layer being lower than an upper surface of the inductor, an upper surface of the ferromagnetic substance layer being higher than the lower surface of the inductor; and

a second metal layer that covers an upper and side surface of the ferromagnetic substance layer, an upper surface of the second metal layer being no lower than the upper surface of the inductor.

15 2. **(Original)** The semiconductor integrated circuit of claim 1, wherein:

the ferromagnetic substance layer is divided into a plurality of parts that are separate from one another when viewed from the direction perpendicular to a surface of the substrate.

3. **(Original)** The semiconductor integrated circuit of claim 1, further including:

20 a multilayer interconnection layer on the substrate; and

the inductor and a laminated film are formed on an uppermost layer of the multilayer interconnection layer, the laminated film comprising the first metal layer, the ferromagnetic substance layer, and the second metal layer.

4. **(Original)** The semiconductor integrated circuit of claim 1, wherein:

25 the inductor, first metal layer and second metal layer comprise a metal selected from the group consisting of copper and aluminum.

5. **(Original)** The semiconductor integrated circuit of claim 1, wherein:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

the ferromagnetic substance layer comprises nickel.

6. **(Withdrawn)** A semiconductor integrated circuit, comprising:

an inductor on a substrate; and

a ferromagnetic substance layer that does not overlap the inductor and
5 surrounds a majority of the inductor when viewed from a direction perpendicular
to a surface of the substrate.

7. **(Withdrawn)** The semiconductor integrated circuit of claim 6, wherein:

the ferromagnetic substance layer completely surrounds the inductor when
viewed from the direction perpendicular to the surface of the substrate.

10 8. **(Withdrawn)** The semiconductor integrated circuit of claim 6, further including:

a multilayer interconnection layer provided on the substrate; and
the ferromagnetic substance layer is formed in a layer selected from the
group consisting of the same layer as the inductor and a layer adjacent to the
inductor.

15 9. **(Withdrawn)** The semiconductor integrated circuit of claim 6, wherein:

the ferromagnetic substance layer comprises nickel.

10. **(Withdrawn)** A semiconductor integrated circuit, comprising:

an inductor on a substrate; and

a plurality of separate ferromagnetic substance layers arranged in a radial
20 fashion around a center area of the inductor on a different level than the inductor.

11. **(Withdrawn)** The semiconductor integrated circuit of claim 10, wherein:

each ferromagnetic substance layer has a strip-like shape and is disposed
longitudinally in a direction from the center area of the inductor toward a
periphery of the inductor.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

12. **(Withdrawn)** The semiconductor integrated circuit of claim 10, further including:
a multilayer interconnection layer provided on the substrate; and
the ferromagnetic substance layers are formed in a layer different from and
adjacent to a layer containing the inductor.

5 13. **(Withdrawn)** A semiconductor integrated circuit, comprising:
an inductor formed on a substrate;
an insulator layer the covers the inductor;
a ferromagnetic substance layer formed on the insulator layer over a center
portion of the inductor; and
10 a pad, formed from a same layer as the ferromagnetic substance layer,
situated in a different region of the semiconductor integrated circuit than the
inductor.

14. **(Withdrawn)** The semiconductor integrated circuit of claim 13, wherein:
the ferromagnetic substance layer covers essentially all of the inductor
15 when viewed from the direction perpendicular to a surface of the substrate.

15. **(Withdrawn)** The semiconductor integrated circuit of claim 13, further including:
a multilayer interconnection layer provided on the substrate; and
the ferromagnetic substance layer and the pad are formed on an uppermost
layer of the multilayer interconnection layer.

20 16. **(Withdrawn)** The semiconductor integrated circuit of claim 13, wherein:
the ferromagnetic substance layer comprises nickel.

17. **(Withdrawn)** A method of manufacturing a semiconductor device, comprising the steps of:
forming a first metal layer on a substrate;
selectively forming a ferromagnetic layer on portions of the first metal
25 layer;
forming a second metal layer that covers the ferromagnetic layer;

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

patterning the first and second metal layers to form a lamination film that includes the first metal layer, the ferromagnetic layer, and the second metal layer; and

forming an inductor, that surrounds the lamination film, from at least one of the layers of the lamination film.

18. (Withdrawn) The method of claim 17, further including:

before forming the first metal layer on a substrate,

forming a recessed portion in the surface on which the lamination film is to be formed, the recessed portion having a depth less than the total thickness of the first metal layer and the ferromagnetic layer combined.

19. (Withdrawn) The method of claim 17, further including:

the ferromagnetic layer comprises nickel.

20. (Withdrawn) A method of manufacturing a semiconductor device, comprising:

forming an inductor on a substrate;

forming an insulator layer that covers the inductor;

forming a film of a ferromagnetic substance on the insulator layer;

patterning the film of the ferromagnetic substance to form a ferromagnetic substance layer over a central portion of the inductor; and

forming a pad from the film of the ferromagnetic substance in a region that is not over the inductor.

21. (New) A semiconductor integrated circuit, comprising:

an inductor on a substrate; and

a laminated film beside the inductor wherein

the laminated film having a ferromagnetic substance layer and a metal layer covering the ferromagnetic substance layer.

22. (New) The semiconductor integrated circuit of claim 21, wherein:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

the metal layer having a first layer and a second layer; and
a lower surface of the ferromagnetic substance layer is covered with the
first layer and an upper surface and a side surface of the ferromagnetic substance
layer is covered with the second layer.

5

23. (New) The semiconductor integrated circuit of claim 22, wherein:

the inductor having a laminated structure of the first layer and the second
layer.

10 **24. (New)** The semiconductor integrated circuit of claim 21, wherein:

the metal layer includes a barrier metal layer.

25. (New) The semiconductor integrated circuit of claim 22, wherein:

each of the first layer and the second layer includes a barrier metal layer.

15

26. (New) The semiconductor integrated circuit of claim 21, wherein:

the laminated film formed inside the inductor when viewed from a
direction perpendicular to a surface of the substrate.

20 **27. (New)** The semiconductor integrated circuit of claim 26, wherein:

the ferromagnetic substance layer is divided into a plurality of parts
separated from one another when viewed from a direction perpendicular to a
surface of the substrate.

25 **28. (New)** The semiconductor integrated circuit of claim 21, wherein:

the laminated film is free from overlapping the inductor and surrounds the
inductor when viewed from a direction perpendicular to a surface of the substrate.

29. (New) The semiconductor integrated circuit of claim 21, further including:

30

a multilayer interconnection layer on the substrate wherein the inductor
and the laminated film are formed on an uppermost layer of the multilayer

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

interconnection layer.

30. (New) The semiconductor integrated circuit of claim 21, furthering including:

5 a multilayer interconnection layer on the substrate wherein the inductor
and the laminated film are formed in different layers of the multilayer
interconnection layer from each other.

31. (New) The semiconductor integrated circuit of claim 30, wherein:

10 the laminated film is divided into a plurality of parts separated from one
another; and

the parts are arranged in a radial fashion around a center area of the
inductor.

32. (New) The semiconductor integrated circuit of claim 31, wherein:

15 each of the parts has a strip-like shape and is disposed longitudinally in a
direction from the center area of the inductor toward a periphery of the inductor.

33. (New) The semiconductor integrated circuit of claim 30, further including:

20 a pad formed in a same layer as the laminated film.

34. (New) The semiconductor integrated circuit of claim 33, wherein:

the pad has the same laminated structure as the laminated film.

35. (New) The semiconductor integrated circuit of claim 30, wherein:

25 the laminated film covers essentially all of the inductor when viewed from
a direction perpendicular to a surface of the substrate.